PATENT
P56937

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of :

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Serial No.:	10/764,525	Examiner:	KIM, SUN M.
Filed:	27 January 2004	Art Unit:	2813

For: FLAT PANEL DISPLAY WITH ANODE ELECTRODE LAYER AS POWER SUPPLY LAYER AND FABRICATION METHOD THEREOF

TRANSMITTAL OF CERTIFIED ENGLISH TRANSLATION OF KOREAN PRIORITY

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

Accompanying this transmittal is the certified English translation of Korean Priority Application No. 10-2003-0007288 (total 20 pages) and the Verification Statement for Translation (1 page) for the above-referenced application.

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VERIFICATION OF TRANSLATION

I, Seung-Hee Lee of Suite 1810, Hwanghwa Bldg., 832-7, Yeoksam-dong, Gangnam-gu, Seoul, Republic of Korea hereby declare that I am knowledgeable in the English and Korean languages, and that to the best of my knowledge the attached document is a true and complete English translation of the Korean Patent Application No. 10-2003-0007288.

Dated January 25, 2010

이 승 희

Signature

Translation of Priority Document

THE KOREAN INTELLECTUAL PROPERTY OFFICE

This is to certify that annexed hereto is a true copy from the records of the Korean Intellectual property Office of the following application as filed

Application Number : Korean Patent Application No. 10-2003-0007288

Date of Application : February 5, 2003

Applicant(s) : Samsung SDI Co., LTD.

COMMISSIONER

[ABSTRACT]

[Abstract of the Disclosure]

The present invention relates to a flat panel display capable of preventing inline short between adjacent wirings and voltage drop through power supply line by using pixel electrode layer as a power supply layer, and a fabrication method thereof.

A flat panel display of the present invention comprises a thin film transistor including source/drain electrodes, formed on an insulation substrate; an insulation film formed on the insulation substrate including the thin film transistor and including first and second contact holes for exposing the source/drain electrodes respectively; an anode electrode formed on the insulation film and connected to one of the source/drain electrodes through one of the first and second contact holes; and a power supply layer formed on the insulation film and connected to the other one of the source/drain electrodes through the other one of the first and second contact holes.

[Representative Drawing]

Fig. 2b

[SPECIFICATION]

[Title of the Invention]

FLAT PANEL DISPLAY WITH ANODE ELECTRODE LAYER AS POWER SUPPLY LAYER AND FABRICATION METHOD THEREOF

[Brief Description of the Drawings]

FIG.1A is a plan view of a conventional organic electroluminescent display device;

FIG.1B is a cross sectional view of a conventional organic electroluminescent display device, taken along a line IB-IB of FIG. 1A;

FIG.2a is a plan view of an organic electroluminescent display device according to preferred embodiments of the present invention;

FIG.2B is a cross sectional view of an organic electroluminescent display device taken along a line □B-□B of FIG. 2A; and

FIG.3A and FIG.3B are plan views of an anode electrode of an organic electroluminescent display device according to preferred embodiments of the present invention.

[Detailed Description of the invention]

[Object of the Invention]

[Technical field of the invention and Related Art prior to the Invention]

The present invention relates to a flat panel display, more particularly, to an organic electroluminescent display device capable of preventing inline short and voltage drop by using anode electrode layer as power supply layer and a fabrication method thereof.

Typically, each pixel of an active matrix organic electroluminescent display device includes a switching transistor, a driving transistor, a capacitor and an EL device, and common power (Vdd) is provided to the driving transistor and capacitor from a power supply line. A common power should be uniformly supplied to numerous pixels arranged in a matrix shape to obtain uniform luminance since the power supply line plays a role of controlling current flowing to the EL device through the driving transistor.

A plurality of conductive layers are used in an active matrix organic electroluminescent display device to form gate line and gate electrode, data line, source/drain electrodes and power supply layer, and anode electrode, etc., wherein insulation layers such as gate insulation film, interlayer insulation film and passivation film is interposed between the conductive layers so that the conductive layers are electrically insulated.

FIG. 1A illustrates plan view of a conventional active matrix organic electroluminescent display device.

Referring to FIG. 1A, a conventional active matrix organic electroluminescent display device comprises a plurality of gate lines 110, a plurality of data lines 120 and a plurality of power supply lines 130, and a plurality of pixels connected to the gate lines 110, data lines 120 and power supply lines 130.

Each of the pixels comprises two transistors and one capacitor including an EL device 160 having a pixel electrode 161, a switching thin film transistor 170 connected to corresponding one of the plurality of gate lines 110 and corresponding one of the plurality of data lines 120, a thin film transistor 150 for driving the EL device 160 connected to corresponding one of the plurality of power supply lines 130, and a capacitor 140 for maintaining voltage between gate and source of the thin film transistor 150.

FIG. 1B illustrates cross sectional view taken along a line IB-IB of FIG. 1A. FIG. 1B is a cross sectional view for one pixel and is limited to illustration of the driving thin film transistor 150, the capacitor 140 and the EL device.

Referring to FIG. 1B, a buffer layer 151 is formed on an insulation substrate 100, and the capacitor 140, the thin film transistor 150 and the EL device 160 are formed on the buffer layer 151. The capacitor 140 includes a lower electrode 144 formed on a gate insulation film 153 and an upper electrode 146 formed on an interlayer insulation film 155.

The thin film transistor 150 comprises a semiconductor layer 152 including source/drain regions 152a and 152b, formed on the buffer layer 151; a gate electrode 154 formed on the gate insulation film 153; and source/drain electrodes 156a and 156b formed on the interlayer

insulation film 155 and connected to the source/drain regions 152a and 152b respectively through contact holes 155a and 155b.

The EL device 160 comprises an anode electrode 161 formed on a passivation film 157, an organic emission layer 163 formed on the anode electrode 161 inside an opening part 165, and a cathode electrode 164 formed on a planarization film 162 including the opening part 165.

In a conventional active matrix organic electroluminescent display device, a power supply line 130 is connected to one of source/drain electrodes 156a and 156b of thin film transistor 150, for example, the source electrode 156a and the upper electrode 146 of the capacitor 140 to play a role of controlling current flowing to the anode electrode 161 of the EL device 160 through the thin film transistor 150, wherein the power supply line 130 commonly supplies power voltage (Vdd) to each of a plurality of pixels.

However, there have been problems in that not only generation of voltage difference of power voltage (Vdd) supplied to each of the pixels through the power supply line 130 by voltage drop (IR drop) causes luminance nonuniformity, but also formation position of the power supply line, line width of the power supply line and position and number of pads connected to an external power source have an effect on design and fabrication process of thin film transistor.

Furthermore, the power supply line 130 together with the data line 120 are formed on the interlayer insulation film 155 so that the power supply line 130 is electrically separated from the data line 120110 as illustrated in FIG. 1a, or the power supply line 130 together with the gate line 110 are formed on the gate insulation film 153 so that the power supply line 130 is separated from the gate line.

Therefore, there have been problems that line defects such as inline short 180 are caused between signal lines arranged adjacently to each other since two different signal lines are formed on the same layer.

[Technical Goal of the Invention]

Therefore, in order to solve the foregoing problems of the prior art, it is an object of the present invention to provide a flat panel display capable of preventing line defects such as inline short of adjacent wirings, and a fabrication method thereof.

It is another object of the present invention to a flat panel display capable of obtaining uniformed luminance by preventing voltage drop through power supply line, and a fabrication method thereof.

It is another object of the present invention to a flat panel display capable of improving emission efficiency of an EL device, and a fabrication method thereof.

In order to achieve the foregoing objects, the present invention provides a flat panel display comprising a thin film transistor including source/drain electrodes, formed on an insulation substrate; an insulation film formed on the insulation substrate including the thin film transistor and including first and second contact holes for exposing the source/drain electrodes respectively; an anode electrode formed on the insulation film and connected to one of the source/drain electrodes through one of the first and second contact holes; and a power supply layer formed on the insulation film and connected to the other one of the source/drain electrodes through the other one of the first and second contact holes.

Furthermore, the present invention provides a flat panel display comprising an insulation substrate divided into a plurality of pixel regions and including a plurality of thin film transistors arranged in each of the pixel regions; an insulation film formed on the substrate; a plurality of pixel electrodes formed on the insulation film and connected to the thin film transistors arranged per each of the pixel regions; and a power supply layer formed on the insulation film such that the power supply layer is electrically separated from the plurality of pixel electrodes to supply common power to the plurality of thin film transistors.

In preferred embodiments of the present invention, the power supply layer is formed in a grid shape in which pixel electrode is arranged in each grid, or the power supply layer is formed in a line shape in which the power supply layer is arranged between pixel electrodes arranged in row or column.

Furthermore, the present invention provides a fabrication method of a flat panel display comprising the steps of forming a thin film transistor including source/drain electrodes on an insulation substrate; forming an insulation film on the substrate; forming first and second contact holes for exposing the source/drain electrodes of the thin film transistor by etching the insulation film; depositing an anode electrode material on the substrate; and forming an anode electrode connected to one of the source/drain electrodes through one of the first and second contact holes and a power supply layer connected to the other one of the source/drain electrodes through the other one of the first and second contact holes by etching the pixel electrode material.

In preferred embodiments of the present invention, the anode electrode material is formed of a material whose work function is 4.5 or more, and the anode electrode material is preferably formed of a material having low resistance and high reflectivity. The pixel electrode material is formed of a single film such as Au, Pt, Ni and Cr, or a laminated film such as Ni/Al/Ni, Ag/ITO and Al/ITO.

[Structure and Operation of the Invention]

The present invention will now be described in detail in connection with preferred embodiments with reference to the accompanying drawings. For reference, like reference characters designate corresponding parts throughout several views.

FIG.2A illustrates plan view of an active matrix organic electroluminescent display device according to preferred embodiments of the present invention, and FIG.2B illustrates cross sectional view of the organic electroluminescent display device. FIG.2B is a cross sectional view of an active matrix organic electroluminescent display device, taken along a line □B-□B of FIG.2A and is limited to illustration to a driving thin film transistor, an EL device and a capacitor in a pixel.

Referring to FIG.2A and FIG.2B, an active matrix organic electroluminescent display device comprises a plurality of gate lines 210 formed on an insulation substrate 200, a plurality of data lines 220 formed on the insulation substrate 200 so that the data lines 220 and gate lines 210 cross each other, a power supply line 230 for supplying common power, and a plurality of

pixels connected to the signal lines 210 and 220 and the power supply layer 230.

Each of the pixels comprises a switching thin film transistor 270 connected to corresponding one of the gate lines 210 and corresponding one of data lines 220, a capacitor 240 connected to the power supply line 230 through a via hole 259, a driving thin film transistor 250 connected to the power supply line 230 through the via hole 259, and an EL device 260.

Herein, an insulation layer such as an interlayer insulation film 255 is interposed between the gate lines 210 and data lines 220 so that the gate lines 210 and data lines 220 are electrically separated from each other. An insulation layer such as a gate insulation film 253 and the passivation film 257 is interposed between the power supply line 230 and the gate and data lines so that the power supply line 230 is electrically separated form the gate and data lines 210 and 220.

A fabrication method of an active matrix organic electroluminescent display device of the present invention having the foregoing structure is described as follows.

A buffer layer 251 is formed on an insulation substrate 200, an amorphous silicon film is crystallized into a polysilicon film by performing an ordinary crystallization process such as excimer laser annealing (ELA) process after depositing the amorphous silicon film on the buffer layer 251. A semiconductor layer 252 is formed in an island shape by patterning the polysilicon film.

A gate insulation film 253 is formed on the buffer layer 251 including the semiconductor layer 252 and a gate electrode 254 is formed by patterning a gate electrode material deposited on the gate insulation film 253 after depositing the gate electrode material on the gate insulation film 253. The gate line 210 and the lower electrode 244 of the capacitor 240 are formed at the same time. Source/drain regions 252a and 252b are formed by ion implanting impurities of a predetermined conductivity type, for example, p type impurities into the semiconductor layer 252 after forming the gate electrode 254.

Contact holes 255a and 255b for exposing the source/drain regions 252a and 252b respectively are formed by patterning the interlayer insulation film 255 after depositing the

interlayer insulation film 255 on the substrate 200. Source/drain electrodes 256a and 256b which are electrically connected to the source/drain regions 252a and 252b through the contact holes 255a and 255b, are formed by patterning a source/drain electrode material after depositing the source/drain electrode material on the interlayer insulation film 255 including the contact holes 255a and 255b. At this time, the data lines 220 and the upper electrode 246 of the capacitor 240 which is overlapped with the lower electrode 244 and connected to the source electrode 256a are formed at the same time so that the driving thin film transistor 250 and capacitor 240 are formed. Although it is not illustrated in FIG.2B, the switching transistor 270 is formed during fabrication process of the driving thin film transistor 250.

The via hole 258 for exposing one of the source/drain electrodes 256a and 256b, for example, the drain electrode 256b and the via hole 259 for exposing the other one of the source/drain electrodes 256a and 256b, for example, the source electrode 256a are formed at the same time by patterning the passivation film 257 after depositing the passivation film 257 on the substrate 200.

Sequentially, by patterning an anode electrode material after depositing the anode electrode material on the passivation film 257 including the via holes 258 and 259, an island shaped anode electrode 261 connected to the drain electrode 256b of the thin film transistor through the via hole 258 is formed, and a power supply line 230 connected to the source electrode 256a of the thin film transistor 250 and the upper electrode 246 of the capacitor 240 through the via hole 259 is formed at the same time.

The anode electrode 261 and power supply line 230 are formed of a conductive material having larger work function compared with an electrode material for the cathode to be formed in the succeeding process, and they are preferably formed of a conductive material having 4.5 or more of work function. Since the anode electrode 261 and power supply line 230 are formed of the same material, it is preferable to use a material having low resistivity to minimize voltage drop of the power supply line 230 and superior reflectivity to increase reflectivity of EL emission layer to be formed in the succeeding process as the conductive material for the anode electrode 261 and power supply line 230.

For example, the conductive material for the anode electrode 261 and power supply line 230 includes a single film such as Au, Pt, Ni and Cr, and a laminated film such as Ni/Al/Ni, Ag/ITO and Al/ITO.

As described in the above, problems of voltage drop of the power supply line 230 and inline short between the gate line and power supply line, or data line and power supply line can be solved without additional processes by simultaneously forming the power supply line 230 in the process of forming the anode electrode 261.

There has been no alternative but to use a transparent conductive material such as ITO or IZO having a larger resistance than a metallic conductive material since a transparent electrode should be used as an anode electrode in an ordinary organic electroluminescent display device having rear emitting structure. Therefore, it has been impossible to use the transparent conductive material having high resistance as the anode electrode and power supply line at the same time. However, conventional inline short between the gate line or data line and power supply line is prevented by forming the anode electrode 261 and power supply line 230 using a material having low resistance and large work function as an organic electroluminescent display device of the present invention adopts the front emitting structure so that a transparent electrode does not need to be used as the anode electrode 261.

FIG.3A and FIG.3B illustrate plan views of the anode electrode 261 and power supply line 230 according to preferred embodiments of the present invention.

In FIG.3A, the power supply line 230 is formed in a grid shape, and the anode electrode 261 is formed in an island shape inside each grid of the power supply line 230, wherein voltage drop through the power supply line 230 can be reduced further more as power voltage (Vdd) is supplied from four directions (shown in arrow) in case that the power supply line 230 is formed in a grid shape.

In FIG.3B, an island shaped anode electrode 261 is arranged in a matrix shape of column and row, and a line shaped power supply line 230 is arranged between neighboring anode electrodes 261 arranged in column. Herein, although the power supply line 230 can be arranged

not only between the neighboring anode electrodes 261 arranged in column as in FIG. 3A, but also between neighboring anode electrodes 261 arranged in row as in FIG. 3A.

It matters little to choose the power supply line of any structure within the range in which an opening ratio is not influenced since the power supply line 230 is formed on other insulation layer different from the gate lines 210 and data lines 220, for example, the passivation film 257 so that short problems between the power supply line 230 and the gate lines 210 or data lines 220 are excluded in preferred embodiments of the present invention. Therefore, the power supply line 230 is formed not only in a grid and line shaped of FIG. 3A and FIG. 3B, but also in a surface electrode shape in which the power supply line 230 is electrically separated from the anode electrode 261 and connected to the upper electrode 246 of the capacitor 240 and one electrode out of the source/drain electrodes 256a and 256b, for example, the source electrode 256a of the thin film transistor 250 through the via hole 559.

Next, a planarization film 262 is formed on the protection film 557 including the anode electrode 261 and power supply line 230, and an opening part 265 is formed by etching the planarization film 262 so that the anode electrode 261 is exposed. Sequentially, a cathode electrode 264 is formed on the substrate after forming an organic emission layer 263 on the anode electrode 261 of the opening part 265.

According to the foregoing preferred embodiments of the present invention, the anode electrode and power supply line are formed at the same time by using a material having low resistance and high reflectivity so as to reduce voltage drop of the power supply line without additional process, prevent inline shorts between the data line or gate line and power supply line, and improve emission efficiency of the EL device. Furthermore, an organic electroluminescent display device according to preferred embodiments of the present invention has merits in that voltage drop of the power supply line can be reduced more by forming the power supply line in a grid shape.

While the invention has been particularly shown and described with reference to preferred embodiments thereof, it will be understood by those skilled in the art that the foregoing and other changes in form and details may be made therein without departing from the spirit and

scope of the invention.

WHAT IS CLAIMED IS:

1. A flat panel display comprising:

a thin film transistor including source/drain electrodes, formed on an insulation substrate;

an insulation film formed on the insulation substrate including the thin film transistor and including first and second contact holes for exposing the source/drain electrodes respectively;

an anode electrode formed on the insulation film and connected to one of the source/drain electrodes through one of the first and second contact holes; and

a power supply layer formed on the insulation film and connected to the other one of the source/drain electrodes through the other one of the first and second contact holes.

2. The flat panel display according to claim 1, wherein the power supply layer and anode electrode are formed of the same material.

3. The flat panel display according to claim 2, wherein the power supply layer and anode electrode are a material having low resistance and high reflectivity.

4. A flat panel display comprising:

an insulation substrate divided into a plurality of pixel regions and including a plurality of thin film transistors arranged in each of the pixel regions;

an insulation film formed on the substrate;

a plurality of pixel electrodes formed on the insulation film and connected to the thin film transistors arranged per each of the pixel regions; and

a power supply layer formed on the insulation film such that the power supply layer is electrically separated from the plurality of pixel electrodes to supply common power to the plurality of thin film transistors.

5. The flat panel display according to claim 4, wherein the power

supply layer is formed in a grid shape in which pixel electrode is arranged in each grid.

6. The flat panel display according to claim 4, wherein the power

supply layer is formed in a line shape in which the power supply layer is arranged

between pixel electrodes arranged in row or column.

7. A fabrication method of a flat panel display comprising the steps of:

forming a thin film transistor including source/drain electrodes on an insulation substrate;

forming an insulation film on the substrate;

forming first and second contact holes for exposing the source/drain electrodes of the thin film transistor by etching the insulation film;

depositing an anode electrode material on the substrate; and

forming an anode electrode connected to one of the source/drain electrodes through one of the first and second contact holes and a power supply layer connected to the other one of the source/drain electrodes through the other one of the first and second contact holes by etching the pixel electrode material.

8. The fabrication method of a flat panel display according to claim 7, wherein the anode electrode material is formed of a material whose work function is 4.5 or more.

9. The fabrication method of a flat panel display according to claim 8, wherein the anode electrode material is formed of a material having low resistance and high reflectivity.

10. The fabrication method of a flat panel display according to claim 8, wherein the pixel electrode material is formed of a single film such as Au, Pt, Ni and Cr, or a laminated film such as Ni/Al/Ni, Ag/ITO and Al/ITO.

[Drawings]

FIG. 1A

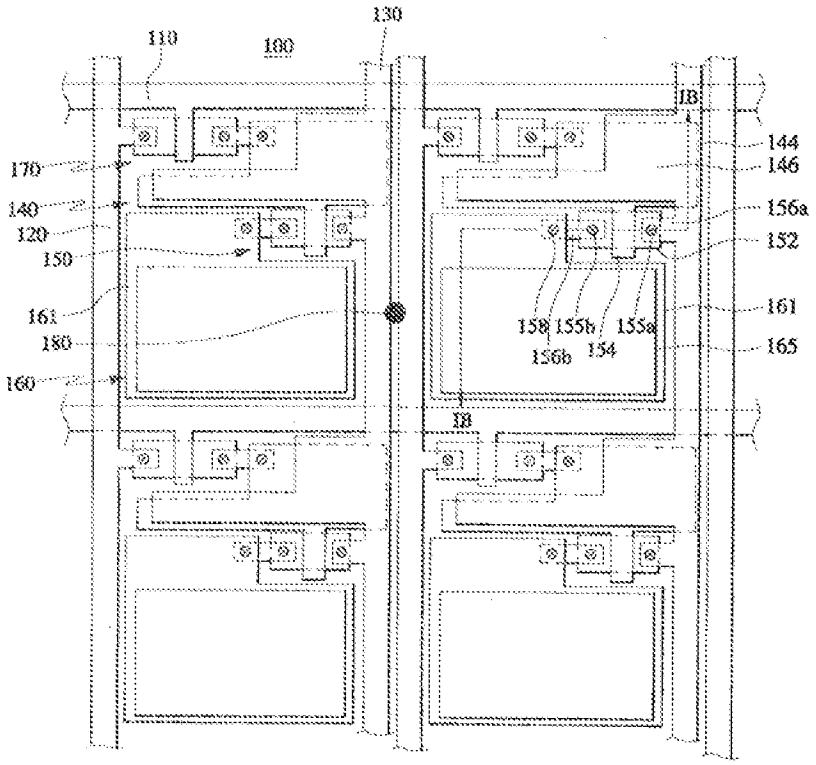

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FIG. 1B

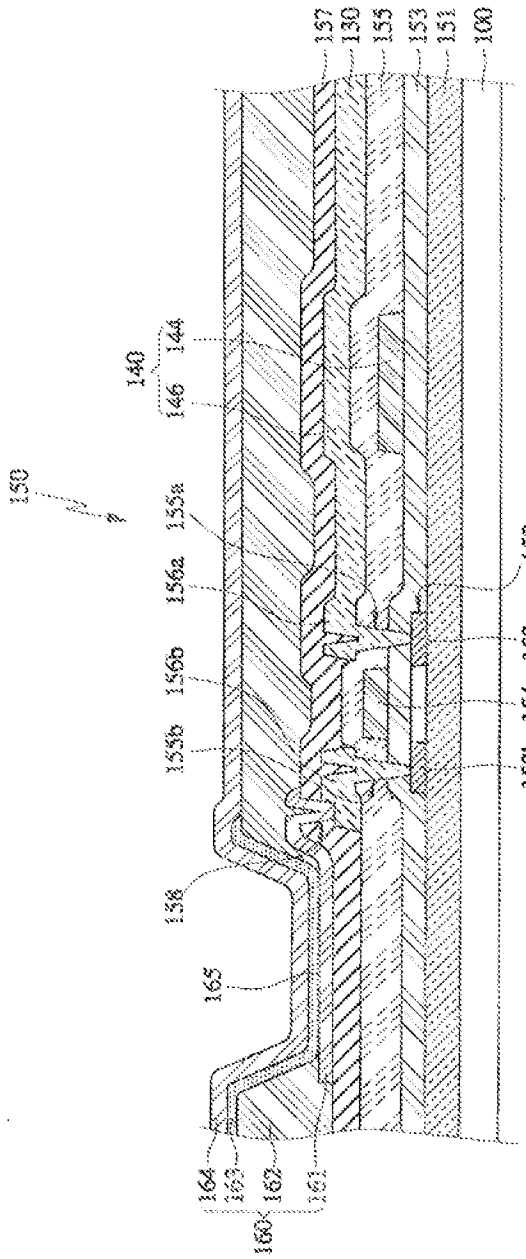
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FIG. 2A

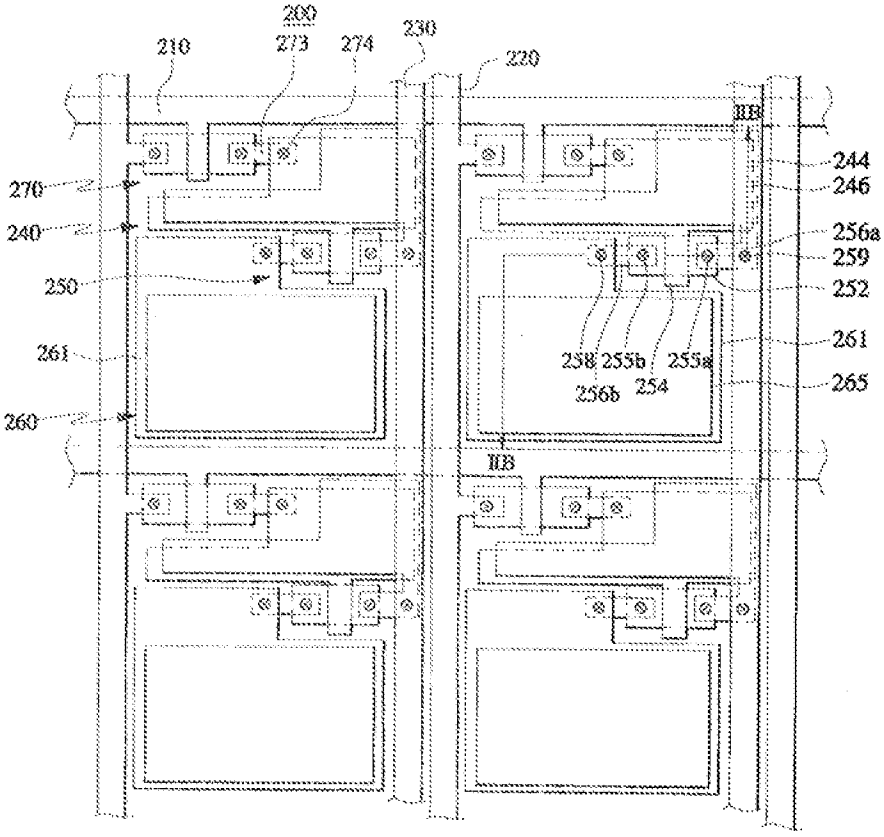
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FIG. 2B

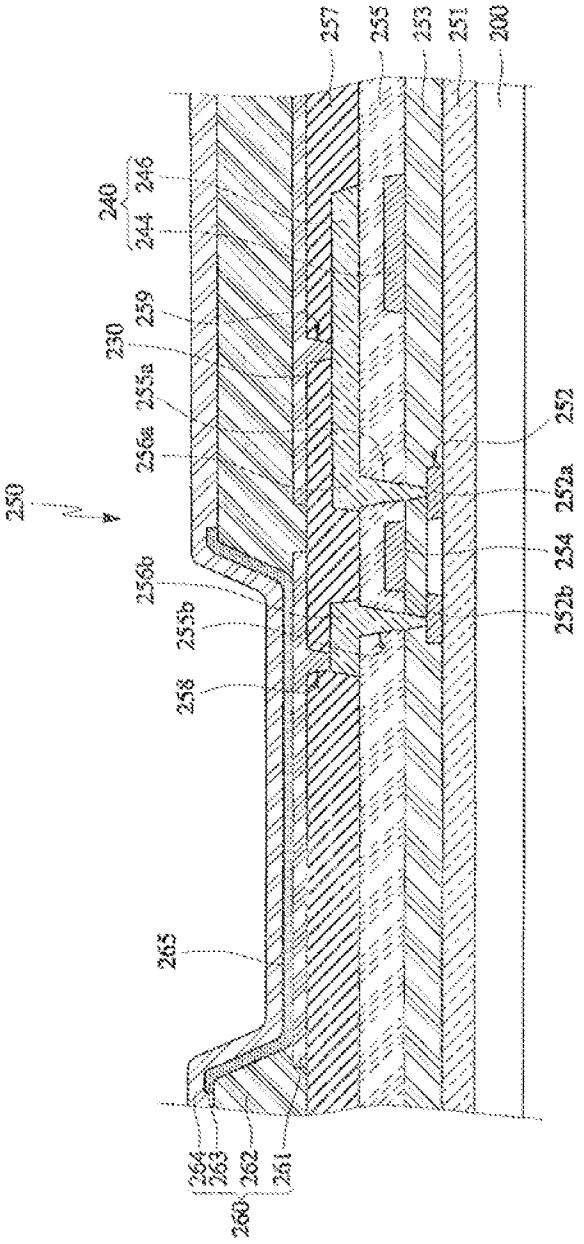
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FIG. 3A

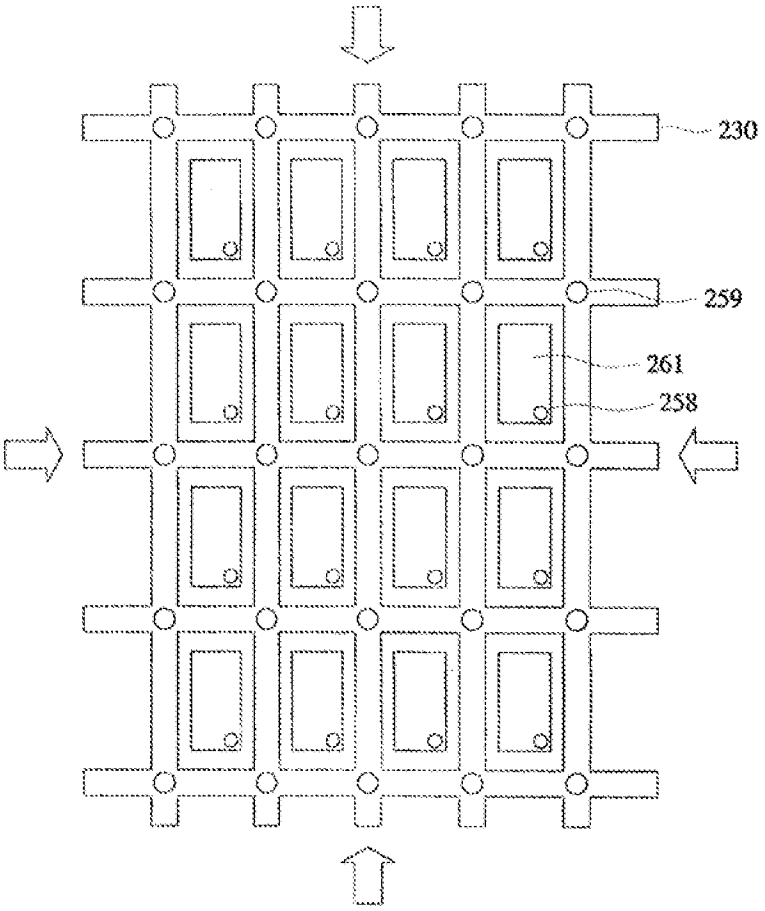

FIG. 3B